IFW

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. BUR920030066US1

In Re Application Of: **METHODS AND APPARATUS FOR DEFECT ISOLATION.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/708380	02/27/04	Unassigned	024241		

Title:

METHODS AND APPARATUS FOR DEFECT ISOLATION.

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☐ the fee set forth in 37 CFR 1.17(p).

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METHODS AND APPARATUS FOR DEFECT ISOLATION.

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

☐ A check in the amount of is attached.

☒ The Director is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below.

- ☒ Charge the amount of
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Robert A. Walsh

Signature

Dated: 7/28/2004

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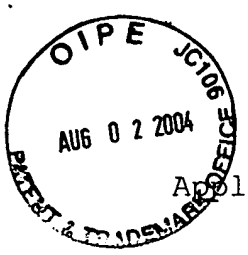

PATENTS
Docket No. BUR920030066US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Leendert M. Huisman, William V. Huott and Franko Motika

Serial No. : 10/708,380

Filed : February 27, 2004

For : METHODS AND APPARATUS FOR DEFECT ISOLATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicants wish to call the attention of the Examiner to the following references:

E.B. Eichelberger, et al., "A Logic Design Structure for LSI Testability", Proceedings of the Fourteenth Design Automation Conference, New Orleans, 1977, pps. 462-468.

David P. Vallett, "IC Failue Analysis: The Importance of Test and Diagnostics", IEEE Design & Test of Computers, July-September 1997, pps. 76-82.

James L. Schafer et al., "Partner SRLS for Improved Shift Register Diagnostics", IEEE VLSI Test Symposium, June 1992, pps. 198-200.

Sandip Jundu, "Diagnosing Scan Chain Faults", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 4, December 1994, pps. 512-517.

Samantha Edirisooriya et al., "Diagnosis of Scan Path Failures", Proceedings of IEEE VLSI Test Symposium April 1995, pps. 250-255.

Sridhar Narayanan et al., "An Efficient Scheme to Diagnose Scan Chains", International Test Conference, July 1997, pps. 704-713.

These references also are listed on the accompanying Information Disclosure Statement (Form PTO-1449). The submission of this Information Disclosure Statement shall not be construed as a representation that a search has been made or that no other art than that identified above exists.

Consideration of the foregoing in relation to this patent application is respectfully requested.

Respectfully Submitted,

Brian M. Dugan, Esq.
Registration No. 41,720
Dugan & Dugan, PC
Attorneys for Applicants
(914) 332-9081

Dated: June 16, 2004
Tarrytown, New York

Sheet 1 of 1 sheet

U.S. Department of Commerce, Patent and Trademark Office	Docket No.: BUR920030066US1	Serial No.: 10/708,380
LIST OF RELEVANT ART CITED BY APPLICANT (Use several sheets if necessary)	Applicant(s): Leendert M. Huisman et al.	
	Filing Date: February 27, 2004	Group: unknown

U.S. Patent Documents

*Examiner Initial		Document Number	Issue Date	Name	Class	Subclass	Filing Date If Appropriate
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
	AG							
	AH							
	AI							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AJ	E.B. Eichelberger, et al, "A Logic Design Structure for LSI Testability", Proceedings of the Fourteenth Design Automation Conference, New Orleans, 1977, pps. 462-468.
	AK	David P. Vallett, "IC Failue Analysis: The Importance of Test and Diagnostics", IEEE Design & Test of Computers, July-September 1997, pps. 76-82.
	AL	James L. Schafer et al. "Partner SRLS for Improved Shift Register Diagnostics", IEEE VLSI Test Symposium, June 1992, pps. 198-200.
	AM	Sandip Jundu, "Diagnosing Scan Chain Faults", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 2, No. 4, December 1994, pps. 512-517.
	AN	Samantha Edirisooriya et al., "Diagnosis of Scan Path Failures", Proceedings of IEEE VLSI Test Symposium April 1995, pps. 250-255.
	AO	Sridhar Narayanan et al., "An Efficient Scheme to Diagnose Scan Chains", International Test Conference, July 1997, pps. 704-713.

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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